Code :R5320404 R5

III B.Tech II Semester(R05) Supplementary Examinations, April/May 2011
VLSI DESIGN
(Electronics & Communication Engineering, Biomedical Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. With neat sketches explain the Ion -lithography process.
2. (a) Explain different forms of pull ups used as load, in CMOS and in enhancement & depletion modes of NMOS.
   (b) Determine the pull up to pull down ratio of an nMOS inverter driven by another nMOS transistor.
3. Design a stick diagram for nMOS EX-NOR gate.
4. Explain the following terms
   (a) Sheet resistance (Rs)
   (b) Standard unit of capacitance (Cg)
   (c) Discuss the possible choice of layers in designing a VLSI design.
5. (a) What type of optimizations are made for the combinational adder? Explain them with a neat schematics.
   (b) Draw the basic structure of pipelined serial/parallel multiplier and compare it with ordinary serial/parallel multiplier.
6. (a) Explain the function of 4:1 Mux in PAL CMOS device with the help of I/O structure.
   (b) Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming.
7. (a) What are the different bitwise operators that available in VHDL and write its syntax with suitable examples?
   (b) Explain the method of Circuit simulation for CMOS circuits and name such simulators.
8. (a) What type of defects are tested in manufacturing testing methods?
   (b) What is the Design for Autonomous Test and what is the basic device used in this?
   (c) What type of tests are used to check the noise margin for CMOS gates?

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